REMARKS

At the outset, Applicants thank the Examiner for the thorough review and consideration of the subject application. The Office Action of March 15, 2004 has been received and its contents carefully reviewed.

In the Office Action of March 15, 2004, the Examiner rejected claims 1-6, 8, 9, and 15-17 under 35 U.S.C. §102(b) as being anticipated by Bird (U.S. Pat. No. 5,852,425); rejected claims 10 and 11 under 35 U.S.C. §103(a) as being unpatentable over Bird in view of Yanagi et al. (U.S. Patent No. 6,310,616); and rejected claims 12, 13, and 14 under 35 U.S.C. §103(a) as being unpatentable over Kanbe et al. (U.S. Patent No. 6,151,016) in view of Matsushima et al. (U.S. Pat. No. 6,396,468).

The rejection of claims 1-6, 8, 9, and 15-17 under 35 U.S.C. §102(b) as being anticipated by Bird is respectfully traversed and reconsideration is respectfully requested.

Claim 1 is patentable over Bird in that claim 1 recites a combination of elements including, for example, "scanning the rows of liquid crystal cells in the liquid crystal display device sequentially; and subsequently, resetting each liquid crystal cell of the liquid crystal display device simultaneously." Bird fails to teach, either expressly or inherently, at least these features of the claimed invention. Accordingly, Applicant respectfully submits that claims 2-6, which depend from claim 1 are also allowable over Bird.

Claim 15 is patentable over Bird in that claim 15 recites a combination of elements including, for example, "a plurality of liquid crystal cells arranged in a matrix of rows and columns... and means for simultaneously resetting all of the liquid crystal cells." Bird fails to teach, either expressly or inherently, at least these features of the claimed invention. Accordingly, Applicant respectfully submits that claims 16 and 17, which depend from claim 15 are also allowable over Bird.

In rejecting claims 1 and 15, the Examiner cites Bird as allegedly showing "subsequently [to sequential scanning the rows of liquid crystal cells], resetting each liquid crystal cell of the liquid crystal display device simultaneously (col. 7, lines 62; col. 8, lines 3-5; since the reset voltage Ve (zero voltage reset) is applied to common electrode 15, all pixels are reset simultaneously)." Applicants respectfully disagree.

For example, Bird teaches at column 3, lines 20-2, that

> "the display elements of a row are reset to a predetermined level during a first part of the selection signal applied to the row concerned and prior to said biasing of the TFTs by applying a reset voltage to the column conductors. Thus, the display elements can be reset in a simple manner as part of a row address period with the reset and charging phases of the operating cycle being immediately consecutive...."

At column 6, lines 28-37, Bird elaborates, stating that

> "each LC display element 12 in the row to be addressed is set to a reference voltage immediately prior to transfer of the video data signals to the display elements. This presetting of the LC display elements is effected by switching appropriate voltage on the row and column conductors 18, 19 and the common... electrode 15. This operation occurs each time the row of display elements is addressed and hereafter will be referred to as the resetting phase."

Further, at column 7, line 51 - column 8, line, 5, Bird specifies

> "[t]he selection signal, is denoted by Vghigh and is chosen so that the TFTs can be turned on. For all other, un-selected, rows of TFTs, the circuit 21 provides a gate voltage having a lower value, Vglow, sufficient to ensure that those TFTs do not conduct. The selection signals applied to successive row conductors are temporally separate...
>
> The write operation begins with the reset phase, occupying the period tr, in which, with the row conductor voltage at Vghigh, the TFT is turned on and the display element is set to a reference voltage according to a voltage VcResetp, then applied to the column conductor by the voltage switching circuit 32... During this reset phase, the voltage Ve of the common electrode 15 is held at the same reference level, i.e., zero volts, by the circuit 23."

As evidenced by the actual teachings of Bird cited above, rows of LC display elements 12 within the display area 14 are sequentially reset upon receipt of selection signal Vghigh, reference voltage VcResetp, and voltage Ve, applied to the common electrode 15. Therefore, it is respectfully submitted that Bird fails to teach, expressly or inherently, "resetting each liquid crystal cell of the liquid crystal display device simultaneously," as asserted by the Examiner and as similarly claimed. For at least this reason, Applicants respectfully request withdrawal of the present rejection under 35 U.S.C. § 102(b).

Claim 9 is patentable over Bird in that claim 9 recites a combination of elements including, for example, "voltage selecting means for selecting, in response to an input control

signal... a normal common voltage to be applied to a common electrode... and for selecting, in response to the input control signal, a reset voltage less than the normal common voltage to be applied to the common electrode...." Bird fails to teach, either expressly or inherently, at least these features of the claimed invention.

In rejecting claim 9, the Examiner cites Bird as allegedly teaching "voltage selecting means for selecting, in response to an input control signal, a normal common voltage (Ve high)... and for selecting, in response to the input control signal, a reset voltage (Ve zero volt) less than the normal common voltage...." Applicants respectfully disagree.

Specifically, at column 8, lines 3-6, Bird states "[d]uring this reset phase, the voltage Ve of the common electrode 15 is held at the same reference level, i.e., zero volts, by the circuit 23" while, at column 8, lines 11-14, Bird merely states "[t]his biasing results from the timing and control circuit 23 switching the common electrode 15 to a higher voltage Vehigh via the line 22 in FIG. 1...." It is respectfully submitted, however, that Bird fails to teach, either expressly or inherently, wherein the timing and control circuit 23 outputs the high and low common voltages Ve cited by the Examiner based on the same control signal as required by present claim 9. For at least this reason, Applicants respectfully request withdrawal of the present rejection under 35 U.S.C. § 102(b).

The rejection of claims 10 and 11 under 35 U.S.C. §103(a) as being unpatentable over Bird in view of Yanagi et al. is respectfully traversed and reconsideration is respectfully requested.

Claim 10 is patentable over Bird in view of Yanagi et al. in that claim 10 recites a combination of elements including, for example, "a voltage amplifier for amplifying an input control signal having a specific logical state... the amplified input control signal to be applied to a common electrode of the liquid crystal display device." Neither Bird nor Yanagi et al. teaches or suggests, singly or in combination, at least these features of the claimed invention. Accordingly, Applicant respectfully submits that claim 11, which depends from claim 10 is also allowable over Bird in view of Yanagi et al.

In rejecting claim 10, the Examiner acknowledges Bird fails to disclose "a voltage amplifier for amplifying an input control signal to a common electrode of the liquid crystal display device and, wherein the voltage amplifier outputs a normal common electrode voltage in

an interval when a data voltage is charged and maintained in the liquid crystal cells, and outputs a reset voltage less than the normal common electrode voltage in the reset interval."

While Bird fails to disclose the subject matter acknowledged above by the Examiner, it is respectfully submitted that such subject matter is not recited in claim 10. To reiterate, claim 10 recites a reset circuit including a voltage amplifier for amplifying an input control signal having a specific logical state only in a reset interval, wherein the amplified input control signal is to be applied to a common electrode of the liquid crystal display device. In light of arguments made above with respect to the rejection of claim 9, it is respectfully submitted that Bird also fails to teach or suggest the elements actually recited in claim 10.

Attempting to cure the Examiner-acknowledged deficiency of Bird, the Examiner cites Yanagi et al. as showing "a voltage amplifier for amplifying an input control signal to a common electrode driver (500; see figure 48) of the liquid crystal display device."

Even if Yanagi et al. shows what it is alleged to show, Applicants respectfully submit Yanagi et al. fails to cure the deficiency of Bird with respect to claim 10. Specifically, Yanagi et al. fails to teach or suggest voltage amplifier for amplifying an input control signal having a specific logical state only in a reset interval, wherein the amplified input control signal is to be applied to a common electrode of the liquid crystal display device. Given that neither Bird nor Yanagi et al. teach or suggest the elements recited in claim 10, Applicants respectfully submit a *prima facie* case of obviousness has not been established and respectfully request withdrawal of the present rejection under 35 U.S.C. § 103(a) for at least this reason.

In concluding with the rejection of claim 10, the Examiner states it would have been obvious to "improve upon the drive circuit [of Bird] for a display device, as disclosed by Yanagi" because "[d]oing so would amplify the input control signal and increase the brightness of the display."

According to M.P.E.P. § 2144.02, the rationale to support a rejection under 35 U.S.C. § 103 may rely solely on logic and sound scientific principle. However, when an Examiner relies on a scientific theory, evidentiary support for the existence and meaning of that theory must be provided.

From the Examiner's theory, it appears that improving Bird "as disclosed by Yanagi" would enable one of ordinary skill in the art to "increase the brightness of the display," thus rendering the claimed invention obvious.

Applicants respectfully submit, however, evidentiary support for the existence and meaning of the Examiner's theory outlined above must be, but has not been, provided. In the absence of any evidentiary support, Applicants respectfully submit Bird and Yanagi et al. have merely been combined using the presently claimed invention as a template via improper hindsight reasoning. For at least this reason, Applicants respectfully request withdrawal of the present rejection under 35 U.S.C. § 103(a).

The rejection of claims 12, 13, and 14 under 35 U.S.C. §103(a) as being unpatentable over Kanbe et al. in view of Matsushima et al. is respectfully traversed and reconsideration is respectfully requested.

Claim 12 is patentable over Kanbe et al. in view of Matsushima et al. in that claim 12 recites a combination of elements including, for example, "a shift register... logical OR gates for performing a logical OR operation of an input reset signal and each gate driving signal from the shift register; and level shifters connected individually to outputs of the logical OR gates...." Neither Kanbe et al. nor Matsushima et al. teaches or suggests, singly or in combination, at least these features of the claimed invention. Accordingly, Applicant respectfully submits that claims 13 and 14, which depend from claim 12 are also allowable over Kanbe et al. in view of Matsushima et al.

In rejecting claim 12, the Examiner cites Kanbe et al. as failing to disclose "level shifters connected individually to outputs of the logical OR gates." Attempting to cure the deficiency of Kanbe et al., the Examiner cites Matsushima et al. as teaching "logic gates (NAND gates 1024 (fig. 6) of MUX 3b (fig. 4)) having input to level shifter 3c (fig. 4), see also col. 11, lines 67 to col. 12, line 2.

Applicants respectfully submit, however, that Matsushima et al. fails to cure the deficiency of Kanbe et al. Specifically, even if Matsushima et al. teaches logic NAND gates having input to level shifters, such a teaching fails to cure the deficiency of Kanbe et al. with respect to claim 12, i.e., Matsushima et al. fails to teach or even suggest level shifters connected to outputs of logical OR gates. For at least this reason, Applicants request withdrawal of the present rejection of claim 12 under 35 U.S.C. § 103(a).

In concluding the rejection of claim 12, the Examiner concludes it would have been obvious to "improve upon the erasing device" of Kanbe et al. because "[d]oing so would provide an erasing device for a LCD image which can erase an afterimage quickly while suppressing the

deterioration of the liquid crystal, and to provide a LCD device including such an erasing device."

It is respectfully submitted that, even if it would have been obvious to improve upon the erasing device disclosed by Kanbe et al. to "provide an erasing device for a LCD image which can erase an afterimage quickly while suppressing the deterioration of the liquid crystal, and to provide a LCD device including such an erasing device," the Examiner has failed to establish that such improvement may be obtained in light of the claimed combination of elements (i.e., a shift register, logical OR gates performing a logical OR operation of an input reset signal and each gate driving signal from the shift register, and level shifters connected individually to outputs of the logical OR gates). In addition, similar arguments presented above with respect to the Examiner's theory of improving Bird in the rejection of claim 10 are equally applicable in the present rejection. For at least these reasons, Applicants respectfully request withdrawal of the present rejection under 35 U.S.C. § 103(a).

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

If the Examiner deems that a telephone conversation would further the prosecution of this application, the Examiner is invited to call the undersigned at (202) 496-7500.

If these paper are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Dated: June 3, 2004

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